

FIG. 1
(PRIOR ART)

Address ...		0	1	2	3	4	5	6	7	
							"1"		"0"	
							↑	↑		
							"1" degeneration	"0" degeneration		
Data pattern	1) 10101010	1	0	1	0	1	"1"	1	"0"	→ 1 bit error detection
	2) 01010101	0	1	0	1	0	"1"	0	"0"	→ 1 bit error detection
	3) 11111111	1	1	1	1	1	"1"	1	"0"	→ 1 bit error detection
	4) 00000000	0	0	0	0	0	"1"	0	"0"	→ 1 bit error detection

※ Two bits of addresses 5, 7 are defective, but a product is processed as nondefective

FIG. 2 (PRIOR ART)

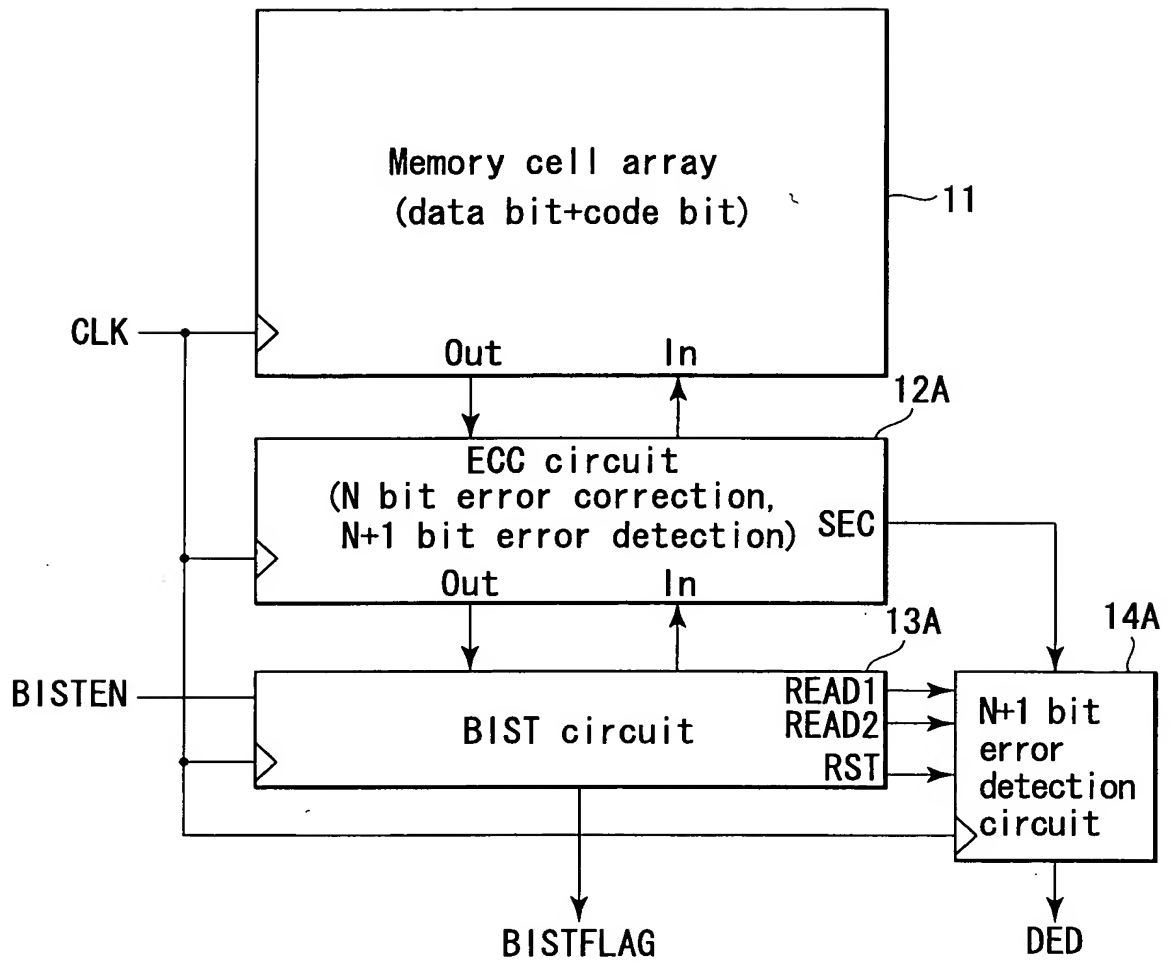


FIG. 3

Test method 1 (in the case of memory on which ECC circuit capable of N bit error correction, N+1 bit error detection is mounted)

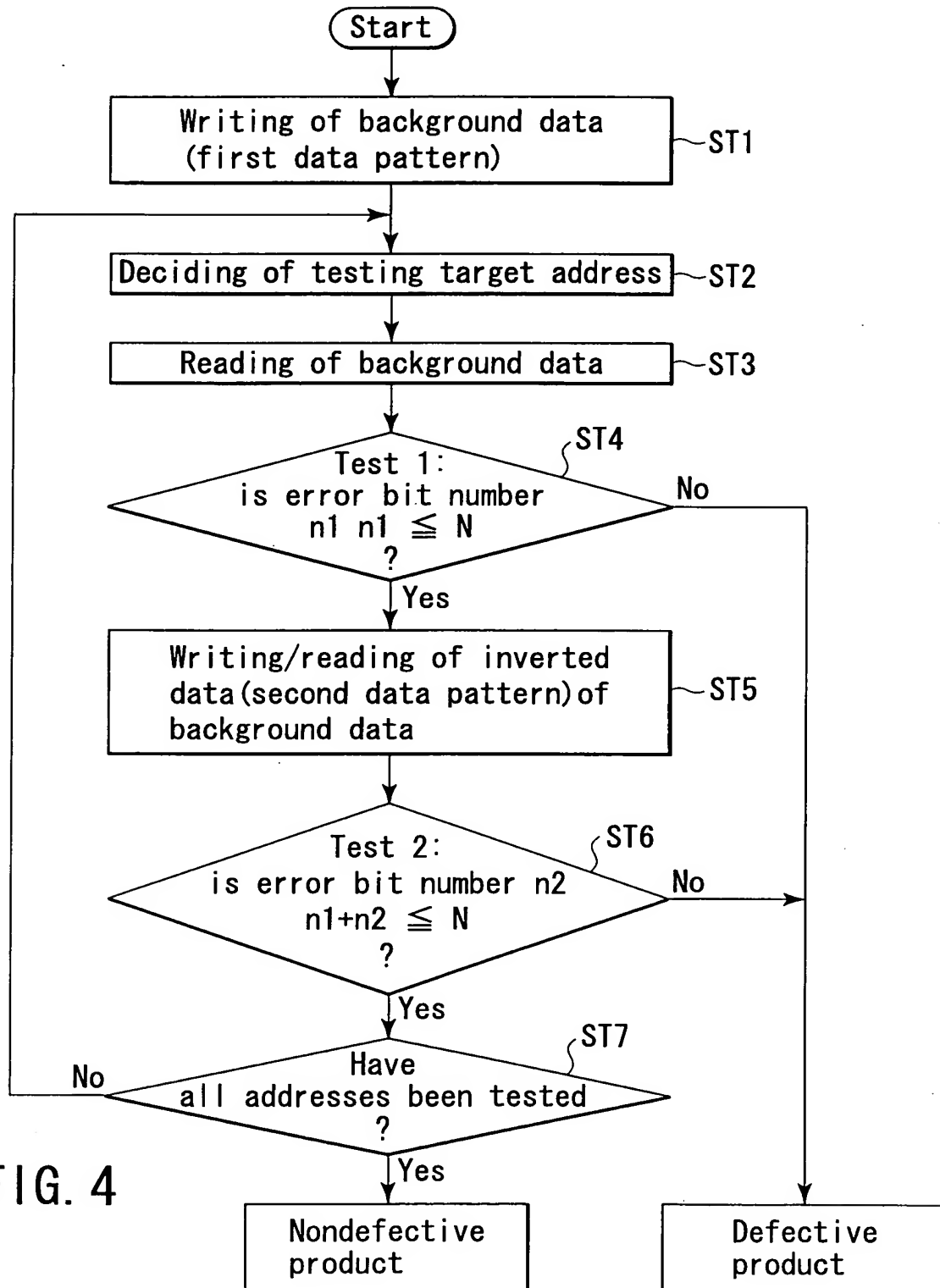


FIG. 4

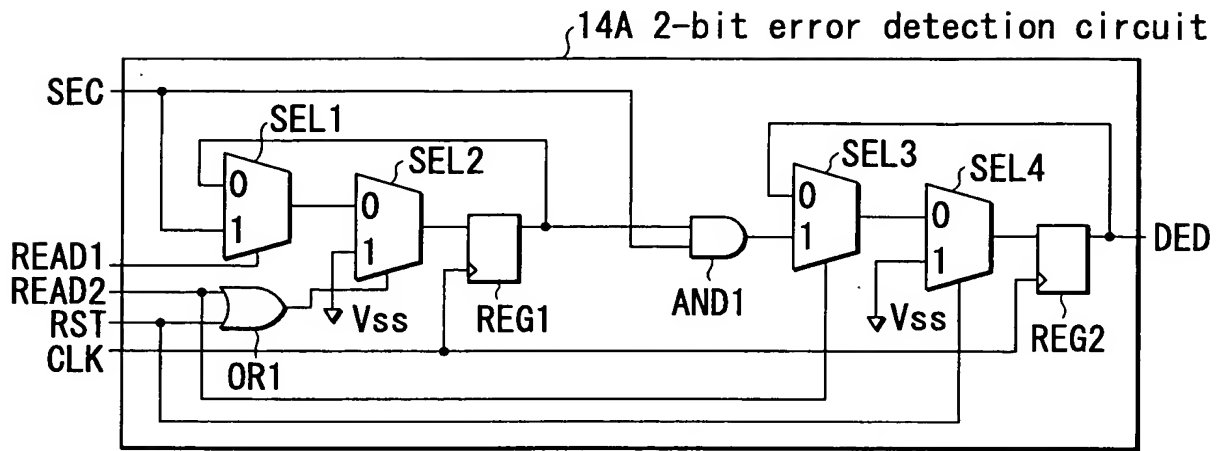


FIG. 5

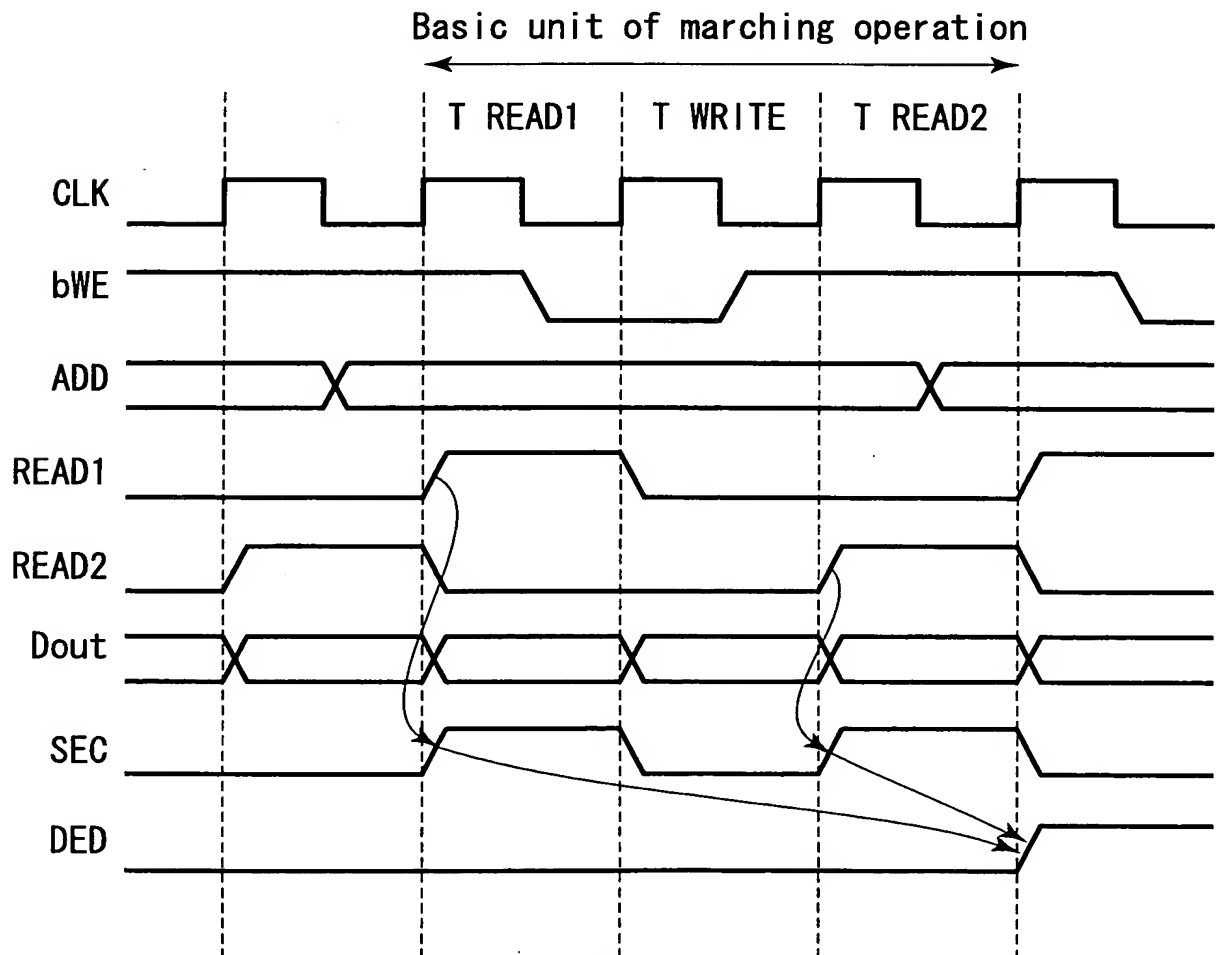


FIG. 6

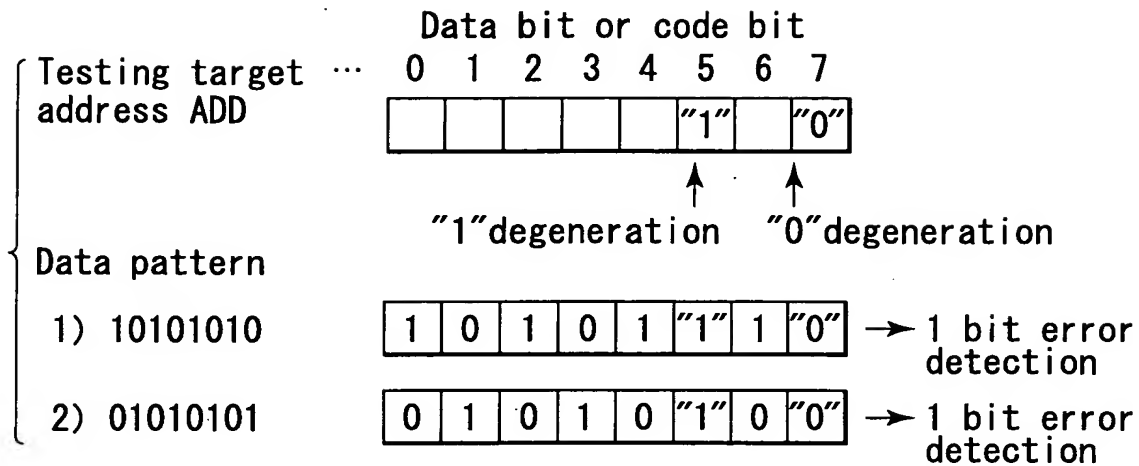


FIG. 7

※ Since two bits of addresses 5, 7 are defective, a product is processed as defective

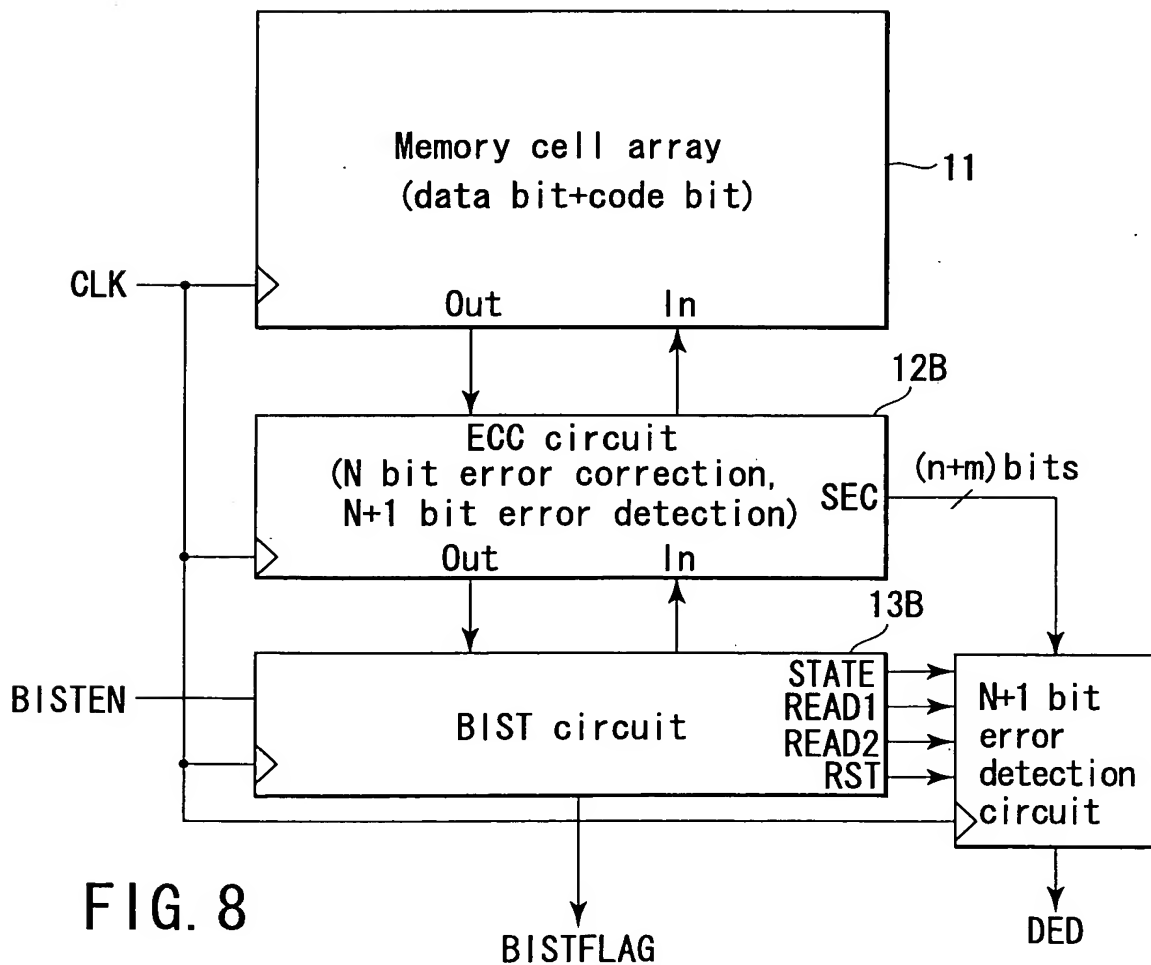


FIG. 8

Test method 2 (in the case of memory on which ECC circuit capable of N bit error correction, N+1 bit error detection is mounted)

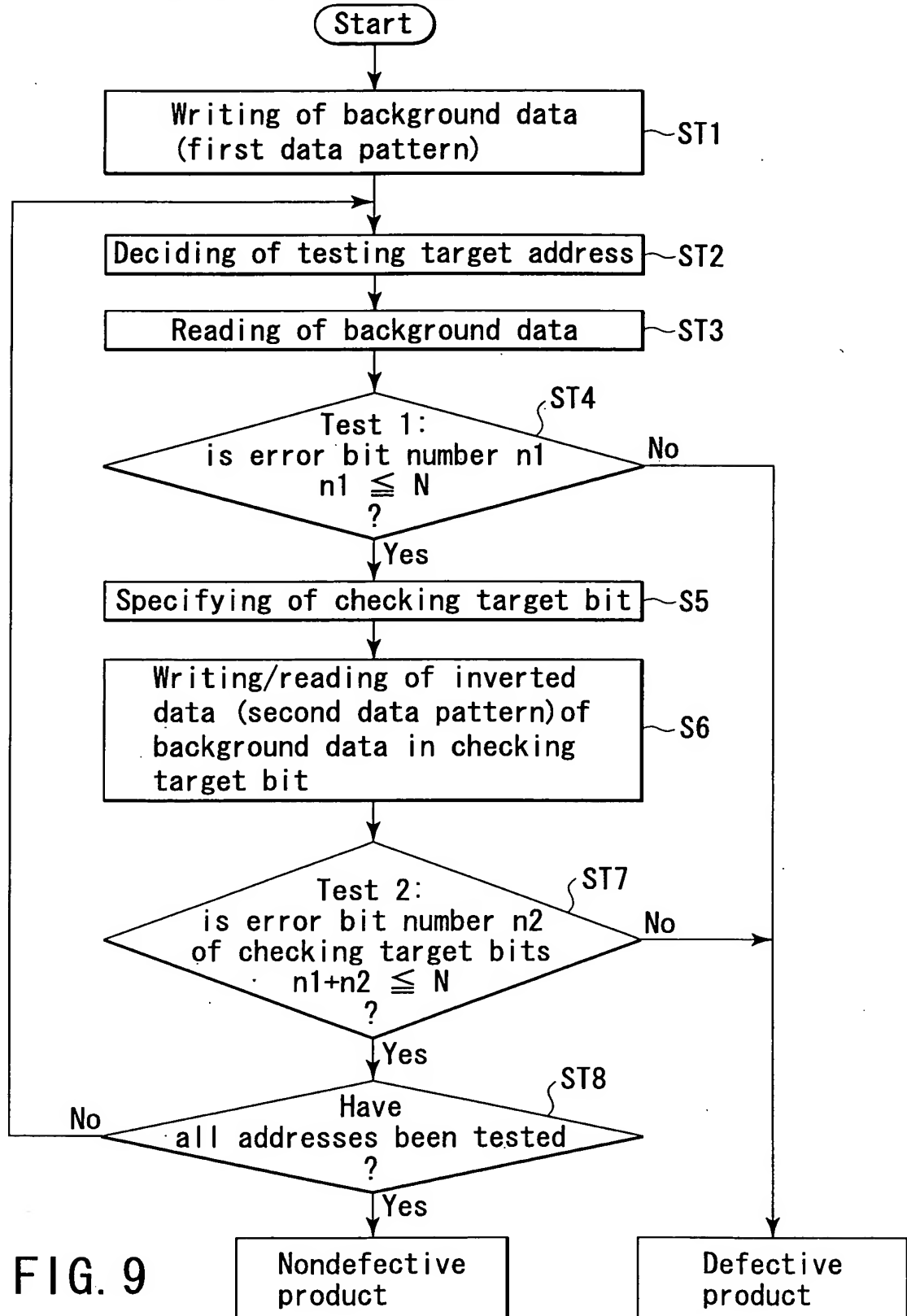


FIG. 9

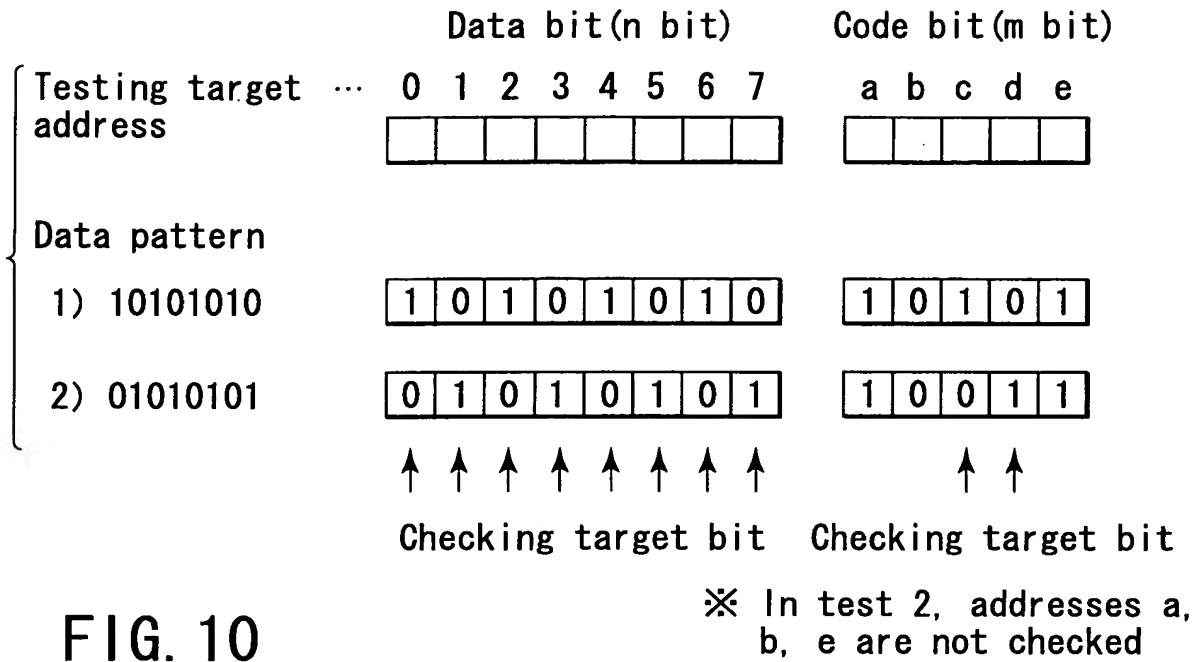


FIG. 10

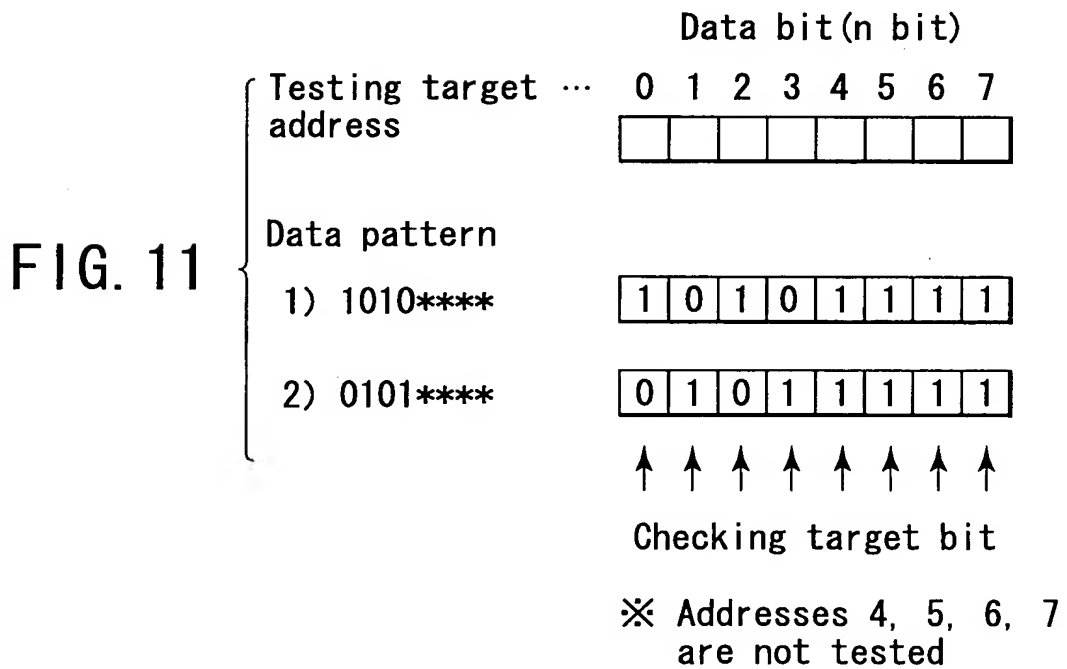


FIG. 11

FIG. 12

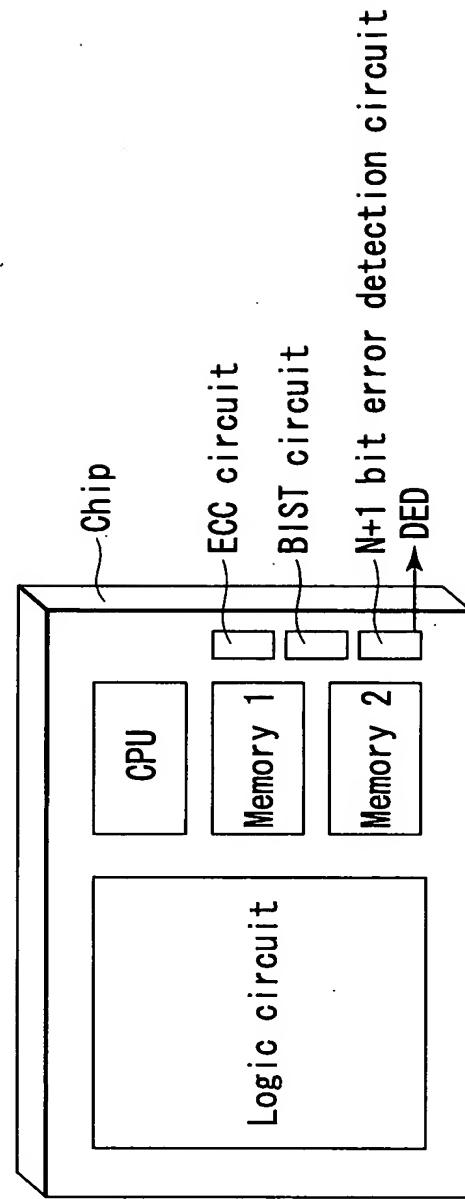
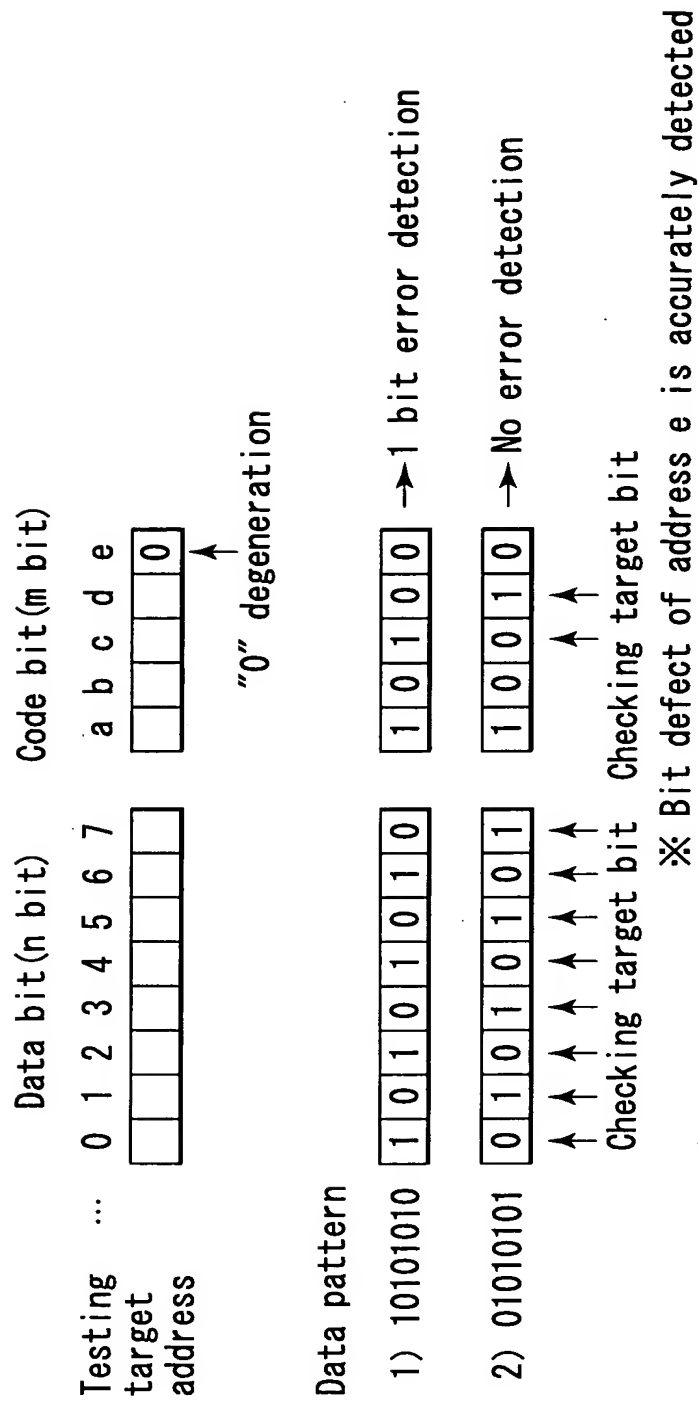


FIG. 13